Test 2 Review

Coverage: Lecture 6, Lecture 7 (Part II only), Lecture 8, related reading assignments, related examples/handouts posted on the lecture page of the course website. Labs 5-7.

Material you can bring: Text books, Freescale manuals, Lecture notes, Example handout, Lab materials. No other material will be allowed.

Format: similar to exam 1.

Restrictions: open book and notes. NO calculator is permitted.

Topics:

Lecture 6 Parallel I/O

(1) The basic bus interface for input/output

Tri-state buffer and latch: operation, important control signal (enable, clock)

(2) Two ways for addressing I/O (pros and cons) and corresponding interface

Memory and I/O both share address bus

Memory mapped I/O: pro: simplify ISA and CPU design; con: memory address space is reduced (address spaces are not overlapped), full address decoding

Separate I/O: pro: cheaper decoder; con: additional control signal (address space overlap), additional instructions

(3) Address decoding (full, partial, linear)

Using discrete logic circuit and 74 series decoder

(4) General bus timing and interface for handshaking I/O

Handshaking using READY (or WAIT)

(5) Multiplexed bus, bidirectional bus and asynchronous bus

Additional control (e.g. strobe, data flow direction, handshaking)

(6) Overview of HC12B32 parallel I/O ports (general purpose vs. special functionality)

Ports A, B, E, S, T, AD
A+B : multiplexed external address and data bus pins (expanded mode)
E: external bus control signal pins (expanded mode)
S: serial communication I/O pins
T: timer I/O pins
AD: ADC input pins

(7) I/O programming model
Data direction registers (input, output, mixture)

(8) Polled I/O

With and without handshaking

(9) HC12B32 expanded mode (narrow vs. wide)

How to use ports A, B, E to create an external bus?
A+B: Address bus
A (or A+B in wide): multiplexed data bus
E: control (E clk, R/W*, LSTRB*)

(10) Aligned/misaligned accesses in expanded wide (16 bit) mode.

Aligned: High byte located at even address
Misaligned: High byte located at odd address
Use A0 (starting address) and LSTRB*(low byte request) to identify different access types: 00

(11) Examples of creating parallel input/output ports in HC12 expanded mode

Input, output, input/output @ even/odd addresses

(12) Examples of interfacing with memory in HC12 expanded mode (narrow vs. wide)

Interface logic design. See HC12 expanded wide mode bus timing analysis example

(13) Timing analysis of HC12 bus expansion

CPU and memory setup and hold time for READ and WRITE operation. See HC12 expanded wide mode bus timing analysis example

Lecture 7 Interrupt

(1) Interrupt vector

How to set interrupt vectors in assembly?

(2) How does CPU response interrupt?

Priority, interrupt acknowledge, multiple interrupts
How is the stack changed before and during ISR execution?
Different between ISR and program subroutine

(3) Enabling interrupt: global vs. local

BSET control_register, enable_bit
CLI

(4) Interrupt priority
How to re-adjust priority?

(5) External interrupt IRQ* and XIRQ* (also see the posted interrupt example)

How to enable? Different sensitivity mode (edge vs. level)

(6) Different way for waiting interrupt

Spin loop/WAI/STOP (implication and overhead)

Lecture 8 Timer

(1) Overview of HC12B32 timer

(2) TCNT, prescale factors

Enabling timer: TEN

Load TCNT value: ldd

(3) Timer overflow (also see the posted TOF example)

How to compute overflow delay?
How to enable TOF interrupt?
How to clear TOF flags? (Inside your ISR)
How to create a delay that requires multiple interrupts?
Why TOF is less accurate than OC?

(4) Output compare (also see the posted OC example)

How to configure a port T channel as output compare channel?
OC delay calculation and TC setup, OC interrupt
OC bit operation: disconnected, set, cleared, toggled

(5) Input capture

How to configure a Port T channel as input capture? IC trigger mode and interrupt.

(6) Pulse accumulator (also see the posted pulse accumulator example: event counting and gated accumulator modes)

Event counting (quantity) mode vs. Gated accumulator (duration) mode
PA setup (PAEN, PAMOD, PEDGE)
PA flags and interrupts

(7) Alternative clock source for TCNT in HC12

Clock source selection and delay calculation

(8) Real Time Interrupt

How to (a) enable (b) change rate (c) clear flag
Labs 5-7:

All software and hardware work you did for these Labs. You should also have knowledge on various chips (latch, SRAM, LCD module) that we used in these labs.