Dr. Tao Li

EEL 4744C: Microprocessor Applications

Lecture 9

Part 1

Serial I/O

Dr. Tao Li

Reading Assignment

• M&M: Chapter 10

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Introduction

• Disadvantage of parallel I/O is wire needed for each bit, cable bulky, expensive, and susceptible to reflections and induced noise leading to limit of short distances

• Serial I/O sends 1 bit @ a time, reducing cost, transmission line effects, and noise problems

• Basic serial comm. system

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Data Coding and Transmission

• Any data code agreeable to both ends will work (e.g. ASCII)

• Two choices for transmission order, UARTs typically send LSB of data first

• Data sent asynchronously, i.e. sent at any time, not synchronized with any process

• Data rate specified in bits/second (e.g. baud rate)

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Standards for Serial I/O Interface

• Define interface between 2 UARTs
  – Standards needed to allow different vendor devices to work

• Key elements defined:
  – Handshaking signals
  – Signal flow direction
  – Communication device types
  – Connectors and interface mechanical issues
  – Electrical signal levels

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Standards for Serial I/O Interface

- Most common standard is RS-232-C
- Signals in RS-232 interface other than for transmitted and received data are for handshaking
- 3 ways data can be sent in serial (simplex, half-duplex, and full-duplex)

Handshaking /w RTS/CTS Signals

- Originally for half-duplex systems
- RTS signal asserted by terminal/computer to serial interface when data ready to be sent
- When interface finds other system is not sending data, it asserts CTS back to terminal/computer
- After receiving CTS, sending station begins transmitting

Handshaking /w RTS/CTS Signals

- Half-duplex system with handshaking
- RTS/CTS useful in simplex; e.g. printer sends CTS to host to signify ready for data
- RTS/CTS useful in full-duplex; e.g. flow control so sender does not overflow receiver

Basic Serial Concepts relating to Modem Applications

- Modems called data communications equipment (DCE)
- Attached to terminals or computers called data terminal equipment (DTE)
- Modems convert logic levels (mark or ‘1’, space or ‘0’) to tones and vice-versa

Basic Serial Concepts relating to Modem Applications

- Modem handshaking signals defined in RS-232 standard
  - Ring indicator (RI): tel. co. transmits special tone that rings phone; modem detects
  - Data set ready (DSR): tells DTE that modem (a.k.a. data set) connected to far end
  - Data terminal ready (DTR): DTE tells modem it is ready to operate

- Data carrier detect (DCD): asserted when carrier being generated by modem on the other end; used first in half-duplex system, where:
  - One end wanted to transmit
  - It first asserted RTS
  - Modem checked DCD bit
  - If found asserted, it knew other end was sending
  - When DCD deasserted, CTS was asserted, allowing transmission from DTE

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Modem Handshaking Signals

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Serial Connectors

**RS-232 Connections**

- Data rate, # data bits, parity on/off, parity type, and # stop bits must match on UARTs
- Several types of cable depending upon full or minimal connection, DTE-DTE vs. DTE-DCE
  - Full DTE-DCE cable
  - DTE-DTE null modem cable
  - Minimal three-wire cable
  - Minimal null modem cable

See Figures 10-7 through 10-10 for cable diagrams

**RS-232 Connections**

- RS-232 logic levels are –25 to –3V for mark (logic-1), +3 to +25V for space (logic-0)
- They provide a large noise margin as compared to TTL
- Limited in distance and data rate (e.g. 50ft at 20 Kb/s), other related standards for faster rates and longer distances (RS-423, RS-422, RS-485)

**UARTs**

- Programmable UARTs used in microprocessor-based systems for serial I/O
- Bus interface: input and output

**UARTs**

- Transmit and receive clocks shift data in and out
- Parallel I/O interface connects UART to CPU
- Example: Motorola MC6850 Asynchronous Communication Interface Adapter (ACIA)
MC6850 UART

- 4 UART registers accessible by CPU selected by R/~W and RS (register select):
  - 00: control register
  - 01: transmit data register
  - 10: status register
  - 11: receive data register

**UART control register:** initialized by program; bits to divide tx/rec clocks by factor of 1, 16, or 64, select # of data bytes, type of parity, # of stop bits, and interrupt control

**UART status register:** status/error bits that may either generate interrupts or be polled by s/w:
  - Received data reg. full (set when data transferred from serial input reg. to rec'd data reg., reset when CPU reads data) to see if new data has arrived since last data read
  - Transmit data reg. empty (set when data transferred from transmit data reg. to serial output reg.)
  - RS-232 modem handshaking bits (DCD, CTS)

**Interrupt request output bit (shows state of h/w IRQ)**

**Error bits**
- Framing error? UART detects an invalid stop bit
- Receiver overrun error? when data transferred from serial input reg. to rec'd data reg. before CPU has read last data; s/w not reading data fast enough, and data possibly lost
- Parity error? received character does not match scheme ⇒ error in code word
Flow Control

- **S/W flow control**: a.k.a. XON/XOFF protocol, XOFF is character (ASCII DC3 typically used, $13$) sent by receiving station to source to stop, and XON is character (ASCII DC1 typically used, $11$) turns on again
  - S/W must detect and generate these characters and act accordingly
  - Can use minimal cable (DTE-DCE or DTE-DTE) as RTS/CTS not needed

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